APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,208	02/09/2001	Hungyu H. Hou	M-9662 US	6979

7590   06/19/2002

Philip W. Woo
SKJERVEN MORRILL MacPHERSON LLP
Suite 700
25 Metro Drive
San Jose, CA   95110-1349

EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.		Applicant(s)	
Office Action Summary	09/780,208		HOU ET AL.	
	Examiner		Art Unit	
	Paresh Patel		2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _04 June 2001_ .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-35_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☒ Claim(s) _1-35_ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _04 June 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)   4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Furuno et al. (US 5444663) in view of Yaklin (US 6157222).

Regarding claim 1 Furuno et al. (hereafter Furuno) discloses : A voltage detector

[fig. 2] comprising:

a voltage following circuit [fig. 4 or 6] connected to a power supply [Vref of fig. 2]

and operable to follow a voltage value of the power supply; and

a switch circuit [fig. 5] coupled to the selectable threshold point circuit [fig. 7] and

the voltage following circuit; the switch circuit cooperating with the selectable threshold

point circuit to generate an output indicating whether the value of the power supply has

increased above or decreased below the selected value for the threshold point in

response to the followed value of the power supply.

Furuno discloses all the essential elements of the claimed invention except for a

selectable threshold point circuit connected to the voltage following circuit and operable

to select one of a plurality of values for a threshold point of the power supply. Yakin

discloses a selectable threshold point circuit [fig. 5 or 7 or 8 or 10] connected to the

voltage following circuit [lines 9-18 of column 2] and operable to select one of a plurality

of values for a threshold point of the power supply [fig. 9]. Rather, Furuno discloses a

supply voltage decision circuit [fig. 7] which outputs a signal corresponding to the input

supply voltage. However, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to provide voltage detector of Furuno with the

selectable threshold point circuit of Yaklin in order to provide a constant voltage to an

internal circuit of IC during testing/normal operation.

Regarding claim 21, Furuno discloses: A system [fig. 1] comprising:

a memory [see fig. 13];

a microprocessor [see fig. 13] ; and

a voltage detector [fig. 2] coupled to the memory and the microprocessor, the

voltage detector comprising:

a voltage following circuit [fig. 4 or 6] connected to a power supply [Vref of fig. 2]

and operable to follow a voltage value of the power supply; and

a switch circuit [fig. 5] coupled to the selectable threshold point circuit [fig. 7] and

the voltage following circuit; the switch circuit cooperating with the selectable threshold

point circuit to generate an output indicating whether the value of the power supply has

increased above or decreased below the selected value for the threshold point in

response to the followed value of the power supply.

Furuno discloses all the essential elements of the claimed invention except for a

selectable threshold point circuit connected to the voltage following circuit and operable

to select one of a plurality of values for a threshold point of the power supply. Yakin

discloses a selectable threshold point circuit [fig. 5 or 7 or 8 or 10] connected to the

voltage following circuit [lines 9-18 of column 2] and operable to select one of a plurality

of values for a threshold point of the power supply [fig. 9]. Rather, Furuno discloses a

supply voltage decision circuit [fig. 7] which outputs a signal corresponding to the input

supply voltage. However, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to provide system of Furuno with the selectable

threshold point circuit of Yaklin in order to provide a constant voltage to an internal

circuit of IC during testing/normal operation.

Regarding claims 2 and 22, Yaklin discloses: the selectable threshold point

circuit is operable to receive a plurality of control signals [element VC1, VC2, VC3 of fig.

5].

Regarding claims 3 and 23, Yaklin discloses: the selectable threshold point

circuit is operable to output a programmable amount of current [fig. 5 and 6].

Regarding claims 4 and 24, Yaklin discloses: the selectable threshold point

circuit comprises a plurality of current mirror transistors [element T21/T20 and T23/T22

of fig. 10].

Regarding claims 5 and 25, Yaklin discloses: at least one of the current mirror

transistors is coupled to a respective switch transistor [element T15 and T16 of fig. 10].

Regarding claims 6 and 26, Yaklin discloses: the switch transistor is operable to

receive a control signal [element V_{CAL} of fig.10].

Regarding claims 7 and 27, Yaklin discloses: the selectable threshold point

circuit comprises a plurality of current mirror transistors, at least two of the current mirror

transistors having a different width-to-length ratio [lines 30-34, 54-58 and 62-65 column 4].

Regarding claims 8 and 28, Furuno discloses: the switch circuit comprises a transistor [elements Q1 or Q2 of fig. 5].

Regarding claims 9 and 29, Furuno discloses: a gate of the transistor [element Q1 of fig. 5] receives the followed value of the power supply [element N1 of fig. 5].

Regarding claims 10 and 30, Yaklin discloses: the switch circuit and the selectable threshold point circuit are connected at a detection node, the switch circuit operable to pull a voltage at the detection node to ground when the value of the power supply is above the selected value for the threshold point [lines 20-22 of column 5 and lines 30-34 of column 6].

Regarding claims 11 and 31, Yaklin discloses: the switch circuit and the selectable threshold point circuit are connected at a detection node, the selectable threshold point circuit operable to pull a voltage at the detection node up to the value of the power supply when the power supply is below the selected value for the threshold point [lines 22-25 of column 5 and lines 35-38 of column 6]. .

Regarding claims 12 and 32, Furuno discloses: a current source generator block [fig. 3and 2] coupled to the voltage-following circuit and the switch circuit.

Regarding claims 13 and 33, Furuno discloses: the current source generator block comprises: a reference transistor [element Q1 of fig. 3]; and a current mirror transistor [element Q4 and Q5 of fig. 3] coupled to the reference transistor and the switch circuit.

Regarding claims 14 and 34, Furuno discloses: the current source generator block comprises: a reference transistor [element Q14 of fig. 3]; and a plurality of current mirror transistors [element Q4/Q5 and Q11/Q12 of fig. 3] coupled to the reference transistor and the switch circuit.

Regarding claims 15 and 35, Furuno discloses: a voltage level detection circuit [fig. 7] coupled to the selectable threshold point circuit and the switch circuit, the voltage level detection circuit operable to output a signal [element V_{CH} of fig. 2] whether the value of the power supply is above or below the selected value for the threshold point.

Regarding claims 16-20, clearly the above discussed combination of Furuno in view of Yaklin will provide the recited method.
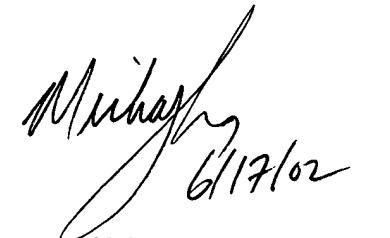

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
June 17, 2002

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800